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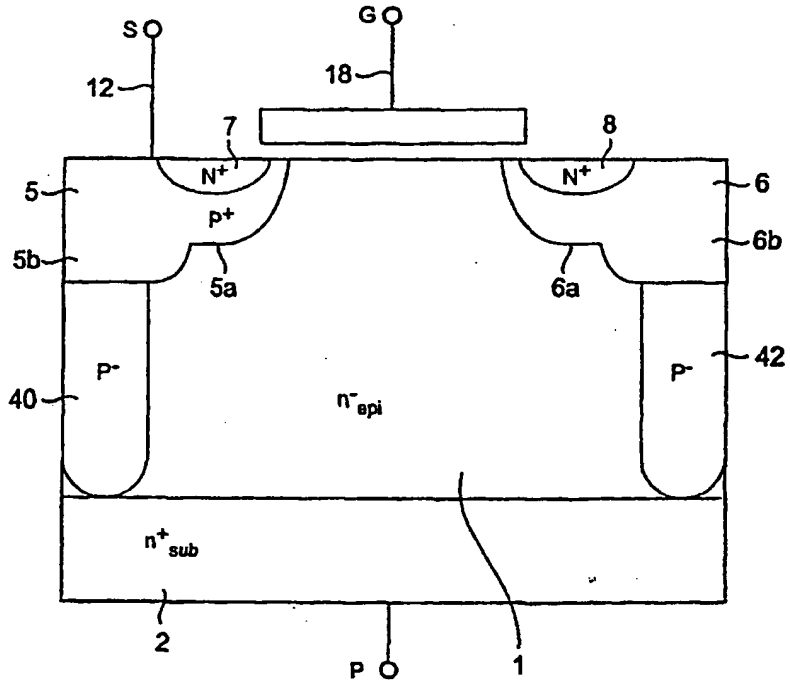
[Continued on next page]

(54) Title: HIGH VOLTAGE POWER MOSFET HAVING LOW ON-RESISTANCE



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

(57) Abstract: A power MOSFET is provided that includes a substrate of a first conductivity type. An epitaxial layer also of the first conductivity type is deposited on the substrate. First and second body regions are located in the epitaxial layer and define a drift region between them. The body regions have a second conductivity type. First and second source regions of the first conductivity type are respectively located in the first and second body regions. A plurality of trenches are located below the body regions in the drift region of the epitaxial layer. The trenches, which extend toward the substrate from the first and second body regions, are filled with a material that includes a dopant of the second conductivity type. The dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches.

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HIGH VOLTAGE POWER MOSFET HAVING LOW ON-RESISTANCE

Related Applications

This application is related to U.S. Provisional Patent Appl. Serial No. _____ entitled "A High Voltage MOS-Gated Structure with a Relatively Low On-Resistance," filed on June 3, 1999.

Field of the Invention

The present invention relates generally to semiconductor devices, and more particularly to power MOSFET devices.

Background of the Invention

Power MOSFET devices are employed in applications such as automobile electrical systems, power supplies, and power management applications. Such devices should sustain high voltage in the off-state and yield low voltage and high saturation current density in the on-state.

FIG. 1 illustrates a typical structure for an N-channel power MOSFET. An N-epitaxial silicon layer 1 formed over an N+ silicon substrate 2 contains p-body regions 5a and 6a, and N+ source regions 7 and 8 for two MOSFET cells in the device. P-body regions 5 and 6 may also include deep p-body regions 5b and 6b. A source-body electrode 12 extends across certain surface portions of epitaxial layer 1 to contact the source and body regions. The N-type drain for both cells is formed by the portion of N-epitaxial layer 1 extending to the upper semiconductor surface in FIG. 1. A drain electrode (not separately shown) is provided at the bottom of N+ substrate 2. An insulated gate electrode 18 comprising oxide and polysilicon layers lies over the channel and drain portions of the body.

The on-resistance of the conventional MOSFET shown in FIG. 1 is determined largely by the drift zone resistance in epitaxial layer 1. The drift zone resistance is in turn determined by the doping and the layer thickness of epitaxial layer 1. However, to increase the breakdown voltage of the device, the doping concentration of epitaxial layer 1 must be reduced while the layer thickness is increased. Curve 20 in FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage for a conventional MOSFET. Unfortunately, as curve 20 shows, the on-resistance of the device increases rapidly as its breakdown voltage increases. This rapid increase in resistance presents a problem when the MOSFET is to be operated at higher voltages, particularly at voltages greater than a few hundred volts.

FIG. 3 shows a MOSFET that is designed to operate at higher voltages with a reduced on-resistance. This MOSFET is disclosed in paper No. 26.2 in the Proceedings of the IEDM, 1998, p. 683. This MOSFET is similar to the conventional MOSFET shown in FIG. 2 except that it includes p-type doped regions 40 and 42 which extend from beneath the body regions 5 and 6 into to the drift region of the device. The p-type doped regions 40 and 42 cause the reverse voltage to be built up not only in the vertical direction, as in a conventional MOSFET, but in the horizontal direction as well. As a result, this device can achieve the same reverse voltage as in the conventional device with a reduced layer thickness of epitaxial layer 1 and with increased doping concentration in the drift zone. Curve 25 in FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage of the MOSFET shown in FIG 3. Clearly, at higher operating voltages, the on-resistance of this device is substantially reduced relative to the device shown in FIG. 1, essentially increasing linearly with the breakdown voltage.

The structure shown in FIG. 3 can be fabricated with a process sequence that includes multiple epitaxial deposition steps, each followed by the introduction of the appropriate dopant. Unfortunately, epitaxial deposition steps are expensive to perform and thus this structure is expensive to manufacture.

Accordingly, it would be desirable to provide a method of fabricating the MOSFET structure shown in FIG. 3 that requires a minimum number of deposition steps so that it can be produced less expensively.

Summary of the Invention

In accordance with the present invention, a power MOSFET is provided that includes a substrate of a first conductivity type. An epitaxial layer also of the first conductivity type is deposited on the substrate. First and second body regions are located in the epitaxial layer and define a drift region between them. The body regions have a second conductivity type. First and second source regions of the first conductivity type are respectively located in the first and second body regions. A plurality of trenches are located below the body regions in the drift region of the epitaxial layer. The trenches, which extend toward the substrate from the first and second body regions, are filled with a material that includes a dopant of the second conductivity type. The dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches, thus forming the p-type doped regions that cause the reverse voltage to be built up in the horizontal direction as well as the vertical direction.

In accordance with one aspect of the invention, the material filling the trench is polysilicon.

In accordance with yet another aspect of the invention, the polysilicon filling the trench is at least partially oxidized. Alternatively the polysilicon may be subsequently recrystallized to form single crystal silicon.

In accordance with another aspect of the invention, the material filling the trench is a dielectric such as silicon dioxide, for example.

In accordance with another aspect of the invention, the material filling the trench may include both polysilicon and a dielectric.

In accordance with another aspect of the invention, a method is provided for forming a power MOSFET. The method begins by providing a substrate of a first conductivity type and depositing an epitaxial layer on the substrate. The epitaxial layer has a first conductivity type. First and second body regions are formed in the epitaxial layer to define a drift region therebetween. The body regions have a second conductivity type. First and second source regions of the first conductivity type are formed in the first and second body regions, respectively. A plurality of trenches are formed in the drift region of the epitaxial layer. The trenches are filled

with a material having a dopant of the second conductivity type. The trenches extend toward the substrate from the first and second body regions. At least a portion of the dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches.

Brief Description of the Drawings

FIG. 1 shows a cross-sectional view of a conventional power MOSFET structure.

FIG. 2 shows the on-resistance per unit area as a function of the breakdown voltage for a conventional power MOSFET and a MOSFET constructed in accordance with the present invention.

FIG. 3 shows a MOSFET structure designed to operate with a lower on-resistance per unit area at the same voltage than the structure depicted in FIG. 1.

FIGs. 4-6 show the pertinent portions of various embodiments of the power MOSFET constructed in accordance with the present invention.

FIG. 7 shows a complete power MOSFET constructed in accordance with the present invention.

Detailed Description

In accordance with the present invention, the p-type regions 40 and 42 shown in FIG. 3 are formed by first etching a pair of trenches that are centered about the position where the p-type regions 40 and 42 are to be located. The trenches are subsequently filled with a dopant rich material. The dopant in the material is diffused out of the trenches and into the adjacent epitaxial layer that forms the drift region of the device. The resulting doped portions of the epitaxial layer form the p-type regions. The material filling the trenches, along with the dopant that has not been diffused out of the trenches, remain in final device. Accordingly, the material should be selected so that it does not adversely affect the characteristics of the device. Exemplary materials that may be used for the material filling the trenches include polysilicon or a dielectric such as silicon dioxide.

FIGs. 4-6 show several different combinations of materials that may be used to fill trenches 44 and 46 that are formed in epitaxial silicon layer 1. While FIGs. 4-6 show the trenches 44 and 46, epitaxial layer 1, and substrate 2, for purposes of clarity FIGs. 4-6 do not show the upper portion of the power MOSFET structure that includes the P-body regions and the sources.

In FIG. 4, the trenches 44 and 46 are filled with a doped dielectric such as boron-doped silicon dioxide. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The boron-doped silicon dioxide that fills the trench remains in the final MOSFET device.

In FIG. 5, the trenches are at least partially filled with polycrystalline silicon, i.e., polysilicon, that is doped with boron. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The remaining boron-doped polysilicon that fills the trench remains in the final MOSFET device. Alternatively, the polysilicon may be all or partially oxidized after the diffusion step is performed to form silicon dioxide. Accordingly, the trench remaining in the final MOSFET device is filled with a dielectric, i.e., silicon dioxide, and any residual polysilicon. In another alternative, any boron-doped polysilicon in the trench is recrystallized at an elevated temperature to form single crystal silicon. In this case the trench remaining in the final MOSFET device is filled with single crystal silicon, or single crystal silicon in combination with silicon dioxide or another dielectric.

In FIG. 6, the trenches 44 and 46 are first partially filled with doped polysilicon followed by the deposition of a dielectric to completely fill the trench. After the trenches are filled, the boron is diffused into the adjacent epitaxial layer 1 to form the p-type regions 40 and 42. The remaining boron-doped polysilicon and the dielectric filling the trench remains in the final MOSFET device. In some cases the boron-doped polysilicon is recrystallized at an elevated temperature to form single crystal silicon. Accordingly, the trench remaining in the final MOSFET device is filled with both single crystal silicon and a dielectric.

FIG. 7 shows the resulting power MOSFET constructed in accordance with the present invention. The MOSFET includes substrate 2, epitaxial layer 1, p-body regions 5a and 6a, deep p-body regions 5b and 6b, source regions 7 and 8, and p-

type regions 40 and 42 in which trenches 44 and 46 are respectively located. Also shown are the gate electrode, which includes oxide layer 48 and polysilicon layer 49, and the source-body electrode, which includes metallization layer 50.

The inventive power MOSFET shown in FIG 7 may be fabricated in accordance with any conventional processing technique. For example, the following series of exemplary steps may be performed to form the power MOSFET depicted in FIG. 7.

First, an oxide masking layer is formed by covering the surface of epitaxial layer 1with an oxide layer, which is then conventionally exposed and patterned to leave mask portions that define the location of the trenches 44 and 46. The trenches are dry etched through the mask openings by reactive ion etching to a depth that typically ranges from 10-40 microns. The sidewalls of each trench may be smoothed. First, a dry chemical etch may be used to remove a thin layer of oxide (typically about 500 – 1000 A) from the trench sidewalls to eliminate damage caused by the reactive ion etching process. Next, a sacrificial silicon dioxide layer is grown over trenches 44 and 46 and the mask portions. The sacrificial layer and the mask portions are removed either by a buffer oxide etch or an HF etch so that the resulting trench sidewalls are as smooth as possible.

The trenches 44 and 46 are filled with any of the previously mentioned materials such as polysilicon, silicon dioxide, or a combination thereof. During deposition, the polysilicon or oxide are typically doped with a dopant such as boron. A subsequent diffusion step is performed to diffuse the dopant out the trenches and into the surrounding epitaxial layer. If the material remaining in the trenches is polysilicon, it may be oxidized or recrystallized.

Next, the N- doped epitaxial layer 1 is grown on a conventionally N+ doped substrate 2. Epitaxial layer 1 is typically 15-50 microns in thickness for a 400-800 V device with a resistivity of 15-60 ohm-cm. The gate oxide is next grown after an active region mask and a layer of polycrystalline silicon is deposited, doped, and oxidized. If employed, deep p-body regions 5b and 6b are formed using conventional masking, ion implantation and diffusion processes. The dose for the deep p-body regions will typically range from about $1x10^{14} - 5x10^{15}/cm^2$. Next, p-body regions 5a and 6a are formed in conventional masking, implantation and

diffusion steps. The p-body regions are boron implanted at 40 to 60 KeV with a dosage froom about $1x10^{13}$ to $5x10^{14}/cm^2$

Next, a photoresist masking process is used to form a patterned masking layer that defines source regions 7 and 8. Source regions 7 and 8 are then formed by an implantation and diffusion process. For example, the source regions may be implanted with arsenic at 80 KeV to a concentration that is typically in the range of $2x10^{15}$ to $1.2x10^{16}/cm^2$. After implantation, the arsenic is diffused to a depth of approximately 0.5 to 2.0 microns. The depth of the deep p-body region typically ranges from about 2.5 to 5 microns while the depth of the body region ranges from about 1-3 microns in depth. Finally, the masking layer is removed in a conventional manner to form the structure depicted in FIG. 7.

The DMOS transistor is completed in a conventional manner by forming and patterning the oxide layer to form contact openings. A metallization layer 50 is also deposited and masked to define the source-body and gate electrodes. Also, a pad mask is used to define pad contacts. Finally, a drain contact layer (not shown) is formed on the bottom surface of the substrate.

It should be noted that while in the previously described process the trenches are formed prior to the formation of the p-body and deep p-body regions, the present invention more generally encompasses processes in which the trenches are formed prior to, or subsequent to, any or all of the remaining doped regions. In addition, while a specific process sequence for fabricating the power MOSFET is disclosed, other process sequences may be used while remaining within the scope of this invention.

The power MOSFET device constructed in accordance with the present invention offers a number of advantages over the prior art device constructed by conventional techniques. For example, the vertical dopant gradient of the p-type regions is very nearly zero. The horizontal dopant gradient may be accurately controlled by varying the amount of dopant that is introduced and the number and duration of thermal cycles used in the diffusion step. Furthermore, the amount of dopant introduced and the lateral dopant gradient can be varied to optimize both the breakdown voltage and the on-resistance of the device.

In the embodiment of the invention shown in FIG. 7 the p-type trench is formed below the body region. However, not every p-type trench need have a body region associated with it, particularly at the perimeter of the die or in regions containing pads or interconnections.

Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention. For example, a power MOSFET in accordance with the present invention may be provided in which the conductivities of the various semiconductor regions are reversed from those described herein.

WHAT IS CLAIMED IS:

1. A power MOSFET, comprising:

a substrate of a first conductivity type;

an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

first and second body regions located in the epitaxial layer defining a drift region therebetween, said body regions having a second conductivity type;

first and second source regions of the first conductivity type respectively located in the first and second body regions; and

a plurality of trenches located below said body regions in said drift region of the epitaxial layer, said trenches being filled with a material having a dopant of the second conductivity type, said trenches extending toward the substrate from the first and second body regions, said dopant being diffused from said trenches into portions of the epitaxial layer adjacent the trenches.

2. The power MOSFET of claim 1 wherein said material filling the trench is polysilicon.

3. The power MOSFET of claim 1 wherein said material filling the trench is a dielectric.

4. The power MOSFET of claim 3 wherein said dielectric is silicon dioxide.

5. The power MOSFET of claim 1 wherein said dopant is boron.

6. The power MOSFET of claim 2 wherein said polysilicon is at least partially oxidized.

7. The power MOSFET of claim 2 wherein said polysilicon is subsequently recrystallized to form single crystal silicon.

8. The power MOSFET of claim 1 wherein said material filling the trench includes polysilicon and a dielectric.

9. The power MOSFET of claim 1 wherein said body regions include deep body regions.

10. A method of forming a power MOSFET comprising the steps of:

providing a substrate of a first conductivity type;

depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type;

forming first and second source regions of the first conductivity type in the first and second body regions, respectively; and

forming a plurality of trenches in said drift region of the epitaxial layer;

filling said trenches with a material having a dopant of the second conductivity type, said trenches extending toward the substrate from the first and second body regions; and

diffusing at least a portion of said dopant from said trenches into portions of the epitaxial layer adjacent the trenches.

11. The method of claim 10 wherein said material filling the trench is polysilicon.

12. The method of claim 10 wherein said material filling the trench is a dielectric.

13. The method of claim 12 wherein said dielectric is silicon dioxide.

14. The method of claim 10 wherein said dopant is boron.

15. The method of claim 11 further comprising the step of at least partially oxidizing said polysilicon

16. The method of claim 11 further comprising the step of recrystallizing said polysilicon to form single crystal silicon.

17. The method of claim 10 wherein said material filling the trench includes polysilicon and a dielectric.

18. The method of claim 10 wherein said body regions include deep body regions.

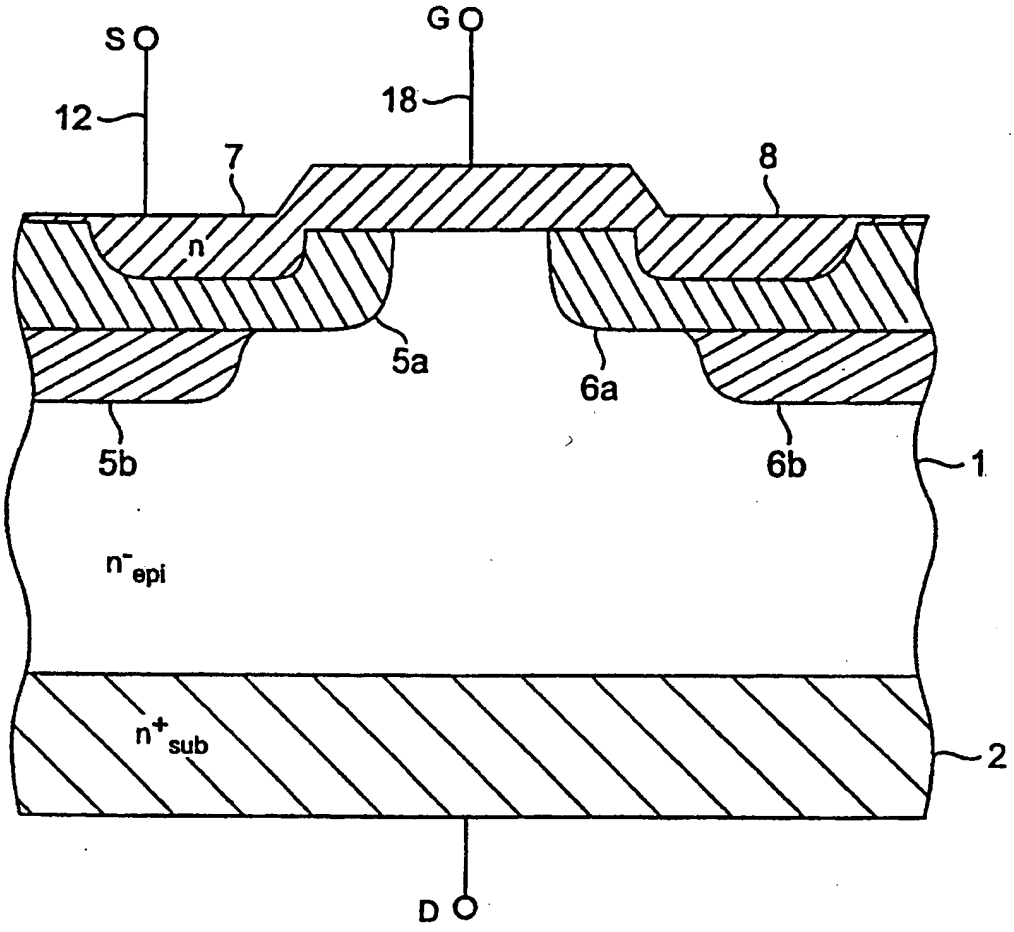
19. The method of claim 10, wherein said trench is formed by providing a masking layer defining at least one trench, and etching the trench defined by the masking layer.

20. The method of claim 10, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

21. A power MOSFET made in accordance with the method of claim 10.

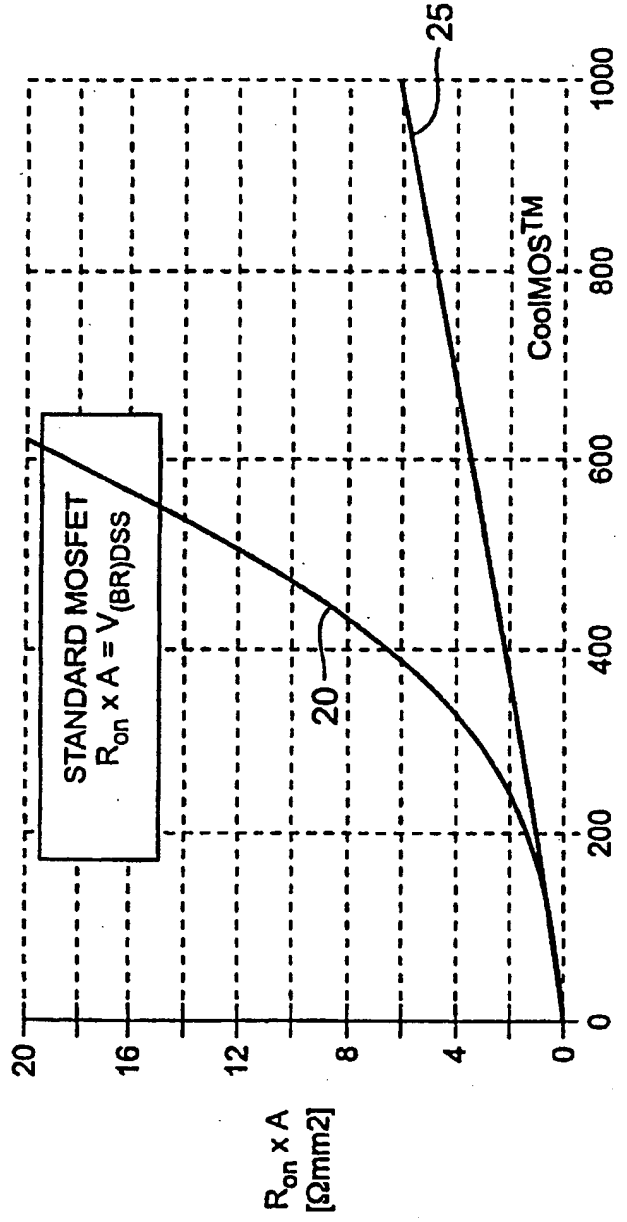
22. The power MOSFET of claim 6 wherein said polysilicon is subsequently recrystallized to form single crystal silicon.

23. The method of claim 15 further comprising the step of recrystallizing said polysilicon to form single crystal silicon.



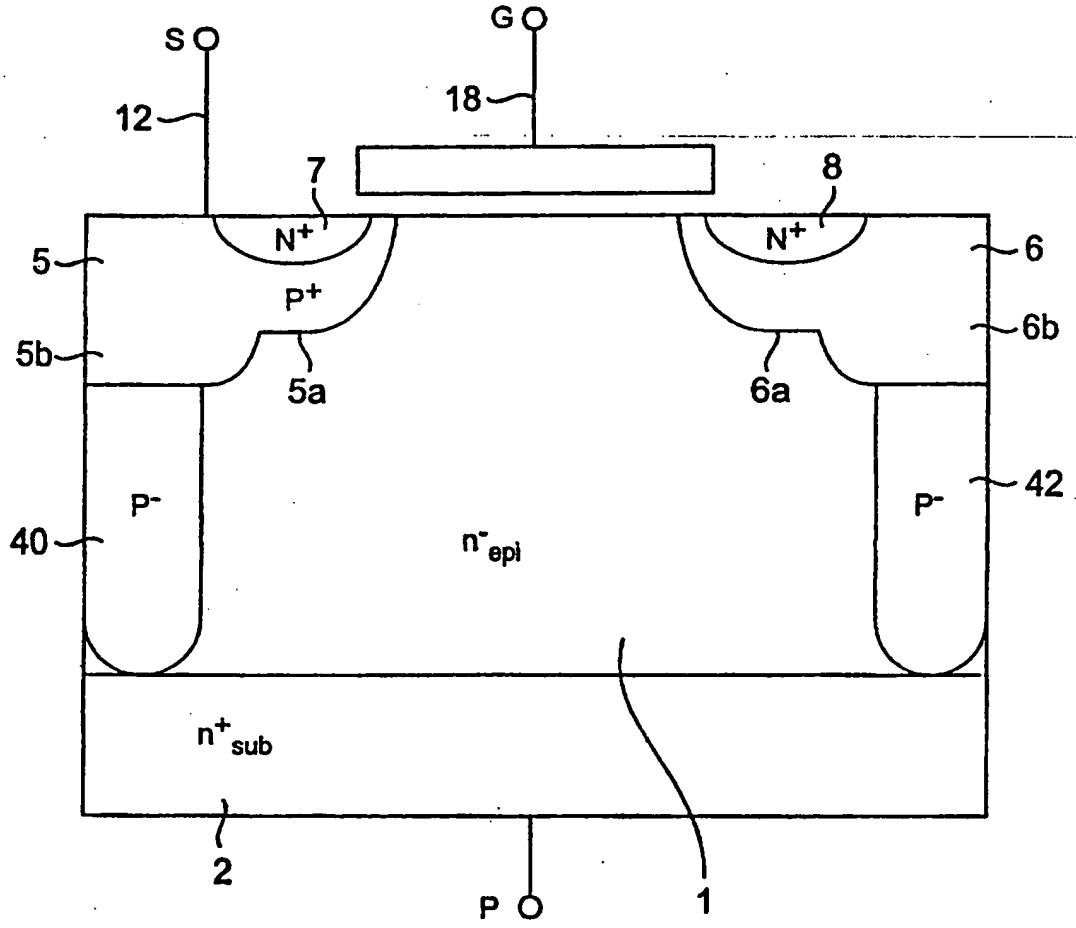
CONVENTIONAL MOSFET

FIG. 1



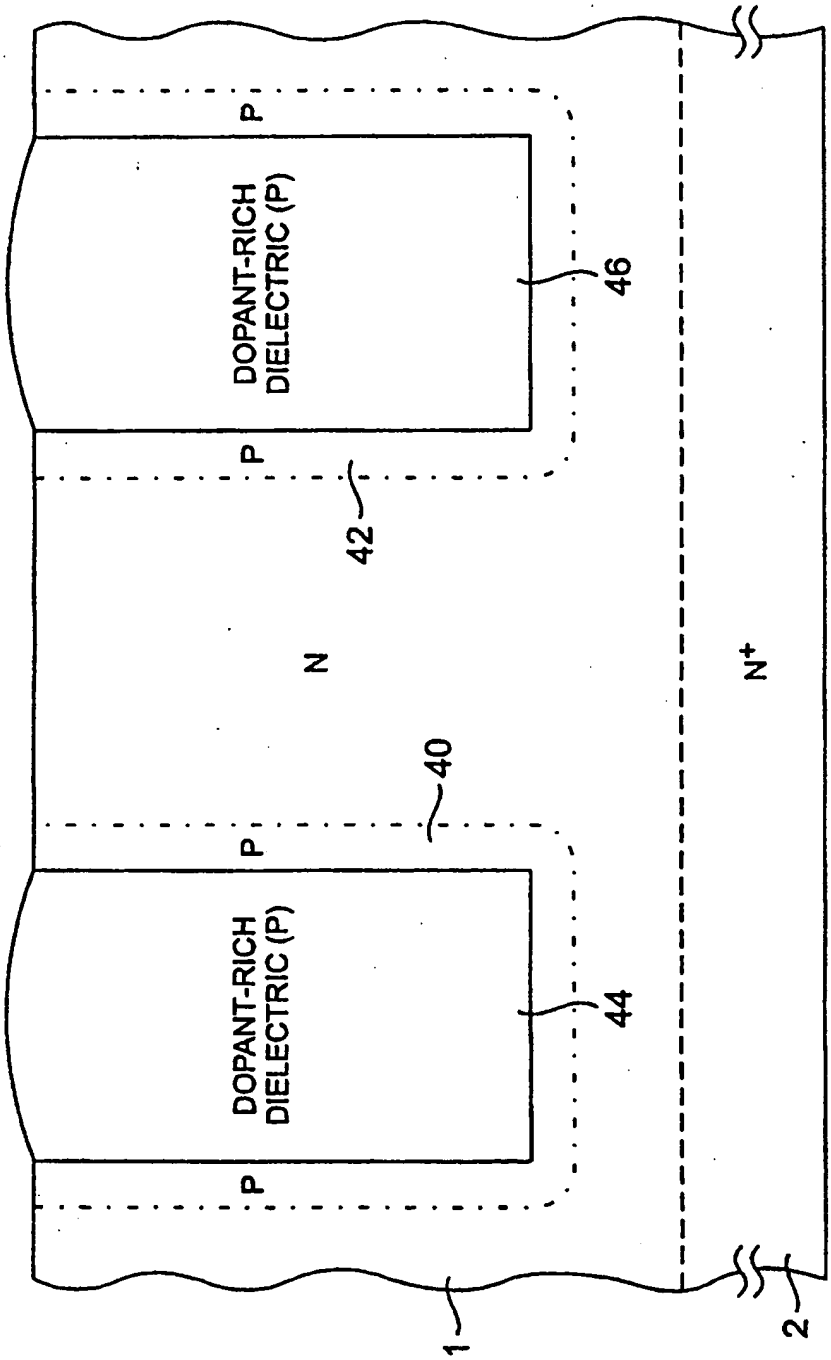
THE SPECIFIC ON-RESISTANCE OF A VERTICAL DMOS TRANSISTOR WITH THE DOPANT DISTRIBUTION OF FIG. 1

FIG. 2



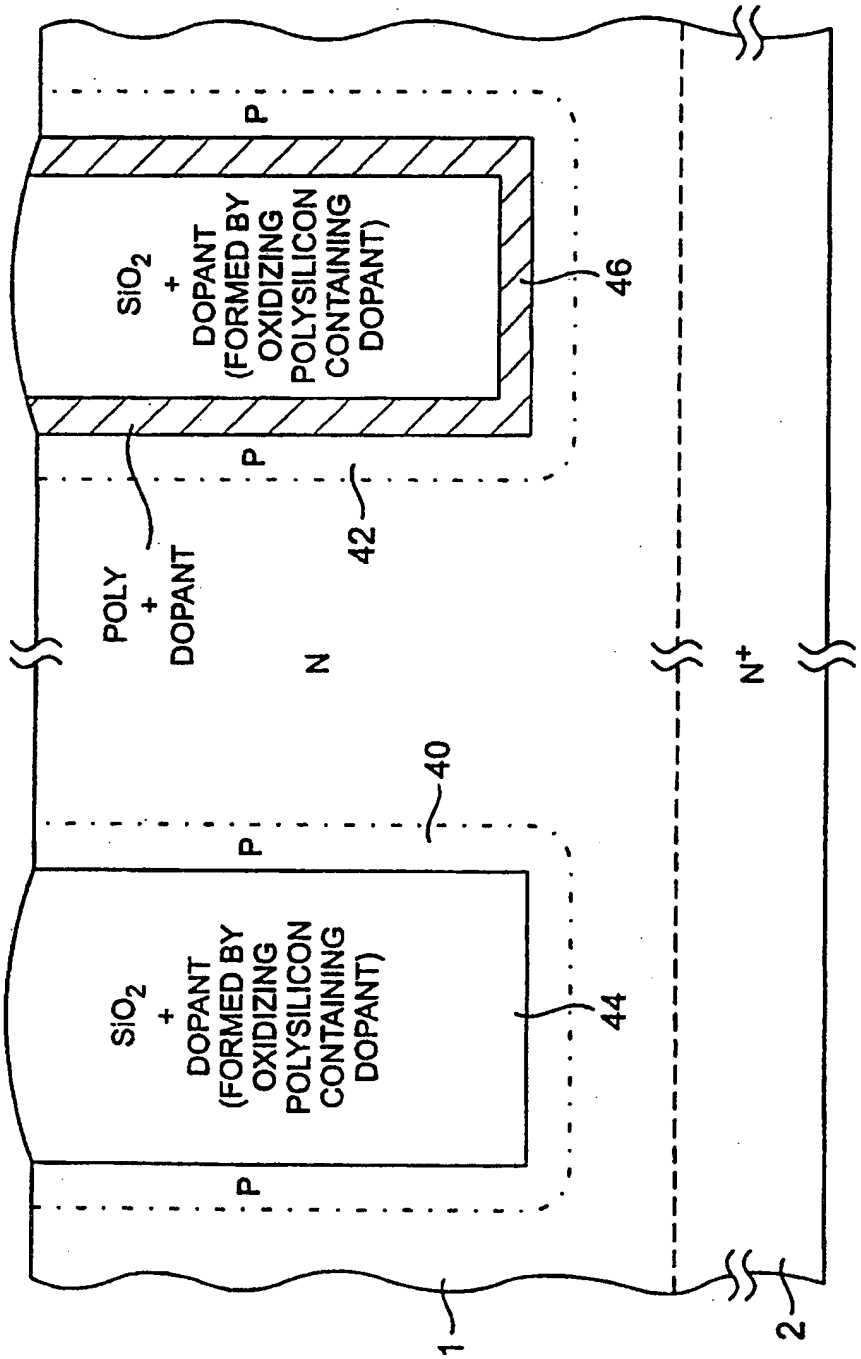
THE DOPANT DISTRIBUTION OF A
HIGH VOLTAGE VERTICAL DMOS TRANSISTOR
WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 3



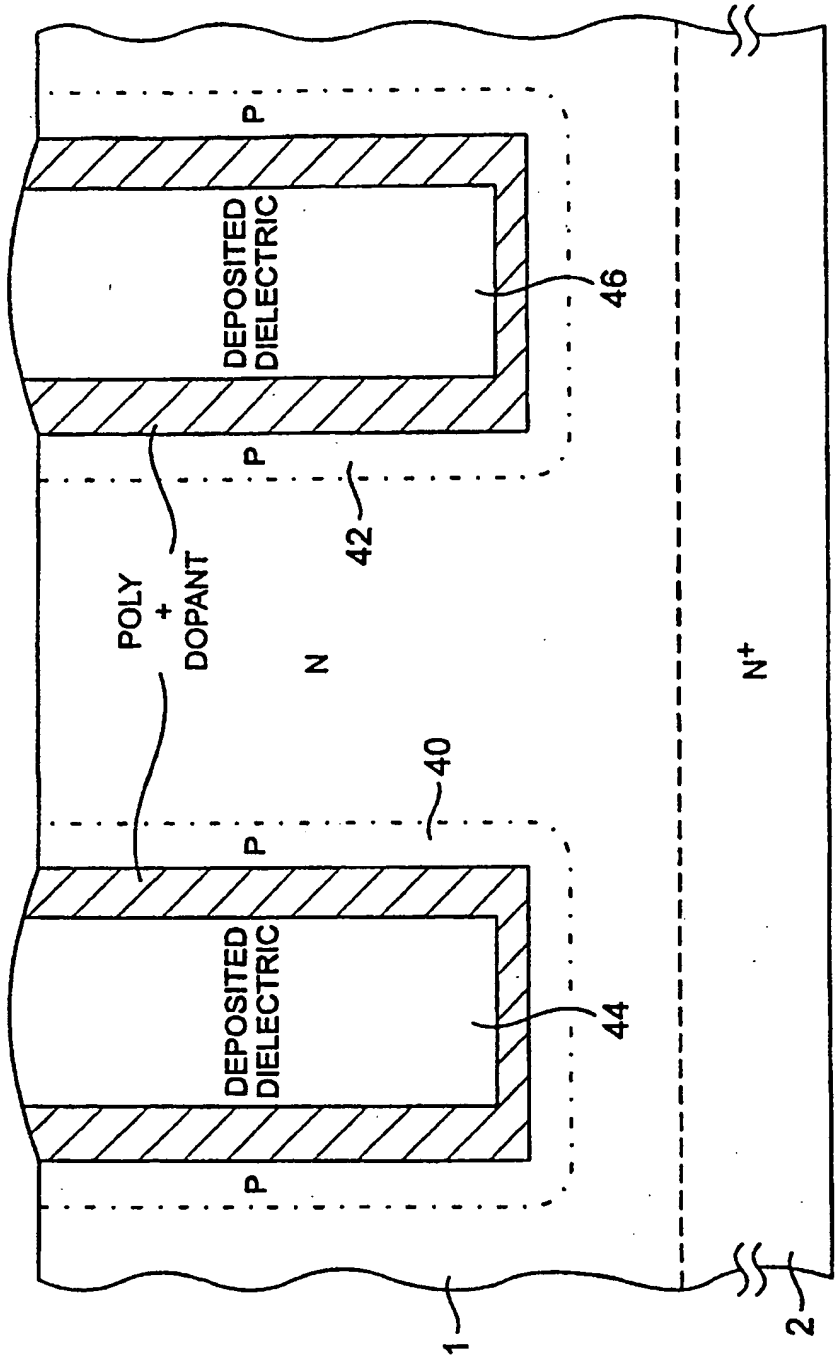
A DOPING PROFILE THAT WAS DIFFUSED FROM TRENCHES FILLED WITH DOPANT-RICH DIELECTRIC

FIG. 4



A DOPING PROFILE THAT WAS DIFFUSED FROM TRENCHES CONTAINING DOPED POLYCRYSTALLINE SILICON THAT WAS SUBSEQUENTLY OXIDIZED

FIG. 5



A DOPING PROFILE THAT WAS DIFFUSED FROM A TRENCH CONTAINING DOPED POLYCRYSTALLINE SILICON AS WELL AS DEPOSITED DIELECTRIC

FIG. 6

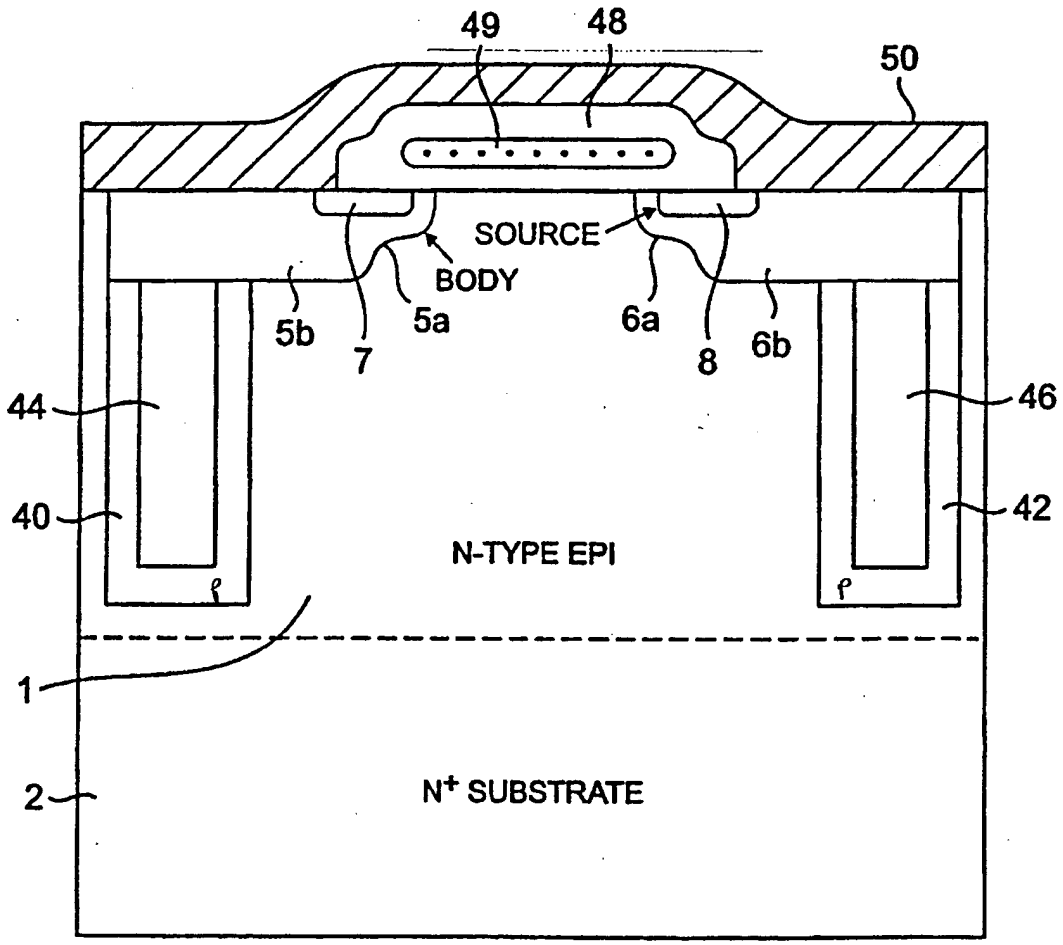

49
48
50
SOURCE
BODY
5b
5a
7
6a
8
6b
44
46
40
42
N-TYPE EPI
1
2
N+ SUBSTRATE

FIG. 7

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(74) Agent: MAYER, Stuart, H.; Mayer, Fortkort & Williams, Suite 250, 200 Executive Drive, West Orange, NJ 07052 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

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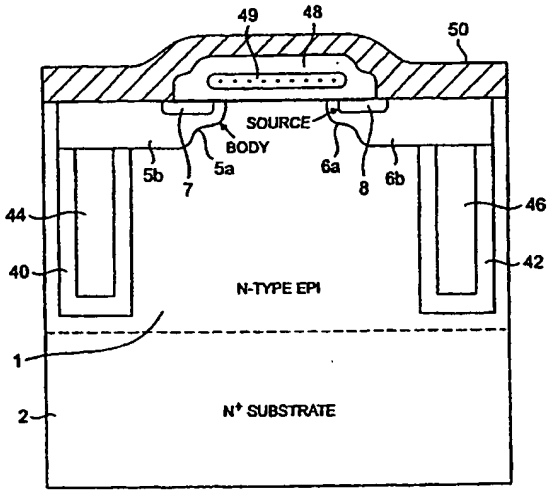
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: POWER MOSFET AND METHOD OF MAKING THE SAME



(57) Abstract: A power MOSFET is provided that includes a substrate (2) of a first conductivity type. An epitaxial layer (1) also of the first conductivity type is deposited on the substrate. First and second body regions (5a, 6a, 5b, 6b) are located in the epitaxial layer and define a drift region between them. The body regions have a second conductivity type. First and second source regions (7, 8) of the first conductivity type are respectively located in the first and second body regions. A plurality of trenches (44, 46) are located below the body regions in the drift region of the epitaxial layer. The trenches, which extend toward the substrate from the first and second body regions, are filled with a material that includes a dopant of the second conductivity type. The dopant is diffused from the trenches into portions of the epitaxial layer adjacent the trenches so as to form semiconductor regions (40, 42) of the second conductivity type under the body regions.

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INTERNATIONAL SEARCH REPORT

Inten nal Application No
PCT/US 00/15189

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L21/336 H01L29/06 H01L21/225

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 216 275 A (CHEN X) 1 June 1993 (1993-06-01)	1,5,7,9, 10,14, 18-21
Y	column 5, line 30 -column 6, line 2; figures 2-5	2,6,8, 11,15-17
Y	CHEN X: "THEORY OF A NOVEL VOLTAGE SUSTAINING (CB) LAYER FOR POWER DEVICES" CHINESE JOURNAL OF ELECTRONICS, vol. 7, no. 3, July 1998 (1998-07), pages 211-216, XP000900759 TECHNOLOGY EXCHANGE LTD, HONG KONG, HK ISSN: 1022-4653 page 215, lines 14-19 of paragraph IV	2,6,8, 11,15-17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 December 2000	28/12/2000

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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/15189

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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